

Create Your First Project

• **Open Vivado**: Launch the Vivado Design Suite.

Step 1: click "Create Project", to create a new project.



Step 2: A wizard for creating a new project will pop up, click "Next"

Vivado 2023.1 Eile Flow Iools New Project		×	- 0	×
AMDE Vivado MLEdition Quick Create Projec Open Examp Tasks Manage IP 3 Open Hardw Vivado Store	Create a New Vivado Project This vitard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.			
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Step 3: In the pop-up dialog box, enter the project name and the directory where the project to be stored. Let's take example of "ps_hello" as a project name. Need to pay attention to the project path "Project location". And click on Next.

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Eile Flow Tools	🍌 New Project					×	
AMD Vivado ML Edition	Project Name Enter a name for y	/our project and specify a directory where the proje	ect data files will be stored.			4	
	Project name:	ps_h ello				0	
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Quici	🗹 Create proje	ect subdirectory					
Create Proje	Project will be c	reated at: C:/Users/User/Desktop/FPGA/ps_hello					
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Step 4: Here we need to select the Project Type. Select "RTL Project" as project type. Then click on Next.



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Step 5: In this window we need to select Target Language and Simulator language, choose "Verilog" as Target Language and "Mixed" as Simulator language then click on "Next"

🏊 Vivado 2023.1			- 0 ×
Eile Flow Tools	New Project	×	
AMD Vivado ML Edition	Add Sources Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.	A	
	+ = + +		
Quich create Projec Open Projec Open Examp Tasks	Use Add Files, Add Directories or Create File buttons below		
Open Hardw	Add Files Add Directories Create File		
Vivado Store	Scan and add RTL include files into project Copy gources into project Add sources from subdirectories Target language: Verilog V Simulator language: Mixed V		
LCarr	? ≤Back Next> Einish C:	ancel	~
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Step 6: Click "Next", do not add any files

Vivado 2023.1 Elle Flow Iools	New Project X	- ¤ ×
AMD Vivado ML Edition	Add Constraints (optional) Specify or create constraint files for physical and timing constraints.	
Quick <u>create Projec</u> Open Projec Open Examp	+, - * *	î
Dopen Hardw Vivado Store	Add Files Qreate File Copy constraints files into project • Back Printin Cancel	ENG 1248 PM
E $\mathcal P$ Type her	re to search 🛛 💼 🗮 💼 💼 💼 🕐 🚾 🔥 🛷	ENG 12-48 PM IN 5/6/2024



Step 7: In this wizard we need select device Family, Package and speed.

- Category: All
- Family: Zynq-7000
- Package: clg400
- Speed: -2
- Temperature: All Remaining
- Static Power: All Remaining

Then click next.



Step 8: Click "Finish" creating the project

Vivado 2023.1 <u>F</u> ile F <u>I</u> ow <u>T</u> ools	🝌 New Project	×] - ¤ ×
		New Project Summary	
Vivado ML Edition	Vivado ML Edition	A new RTL project named 'ps_hello' will be created.	
		O No source files or directories will be added. Use Add Sources to add them later.	
Outicl		O no constraints files will be added. Use Add Sources to add them later.	î
QUICH <u>Create Projec</u> Open Project Open Examp		The default part and product family for the new project: Default Part. xc7z010cj400-2: Family: 7xmq7000 Package: clg400 Speed Grade: -2	
Tasks			
Manage IP >			
Open Hardw			
Vivado Store			
Learr		To create the project, click Finish	
Tcl Console	•	<back next=""> Emph</back>	► Vindows.
Type her	e to search	📘 🗄 💼 💼 💽 🖳 📥 🛷 🛛 💛 33°C Sunny 🔨 단 🚛 4. 5	ENG 12:53 PM IN 5/6/2024



Step 9: Once the Project is created we need to create Block Design. In order to create Block Design please expand Project manager, here expand IP Generator then click on Create Block Design as shown in the image below.



Step 10: Here no modifications can be done, keep the default "design_1"





Step 11: Click "Add IP" as shown in the below image.

ps_hello - [C:/Users/User/Desktop/FP(3A/ps_hello/ps_hello.xprJ - Vivado 2023.1			- D
<u>File Edit Flow Tools Re</u>	p <u>o</u> rts <u>W</u> indow La <u>v</u> out <u>V</u> iew <u>H</u> el	Ip Q- QUICK Access		Ready
		10 ×		E Default Layout
Flow Navigator 😤 🗘 ?	BLOCK DE SIGN - design_1			?
 PROJECT MANAGER Settings 	Sources Design × Signals	? _ 🗆 🖾 Dia	igram	2023
Add Sources	Q X 3	\$ 6		🖈 C 🔄 🗖 Default View 🗸 🕻
Language Templates	🏯 design_1		Add IP (Ctrl+I)	
👎 IP Catalog				
IP INTEGRATOR Create Block Decise			This design is empty. Press the	+ button to add IP.
Create Block Design	Properties	? _ 🗆 🖾 ×		
Open Block Design		$\leftarrow \Rightarrow \phi$		
Generate Block Design	Select an object to	o see properties		
SIMULATION	Tcl Console × Messages Lo	g Reports Design Runs		? _ 🗆 [
Run Simulation	Q			
V RTI ANALYSIS	start_gui			-
Run Linter	INFO: [IP_Flow 19-234] Refr	reshing IP repositories	part MC/2010C1g400-2	
> Open Elaborated Design	INFO: [IP_Flow 19-1704] No	user IP repositories specified	r (Nivada /2022 1/data /in)	
> Open Elaborated Design	create_bd_design "design_1"	"	R/VIVad0/2023.1/data/1p .	
V SYNTHESIS	Wrote : <c:\users\user\des< td=""><td>sktop/FPGA/ps_hello/ps_hello.srcs/s</td><td>ources_l\bd\design_l\design_1.bd></td><td></td></c:\users\user\des<>	sktop/FPGA/ps_hello/ps_hello.srcs/s	ources_l\bd\design_l\design_1.bd>	
Run Synthesis	aparte_oraci inte	see sources_r		
> Open Synthesized Design				Activato Windows
	Type a Tol command here			Go to Settings to activate Windows.
 IMPLEMENTATION 				

Step 12: Here in search icon search for "zynq", double-click "ZYNQ7 Processing System" as shown in the below image.



<u>File Edit Flow Tools Repo</u>	rts <u>Window Layout View H</u> elp <u>Q. Quick Access</u>		Ready
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Language Templates	🟯 design_1	* Designer Assistance available. Run Block Automation	
P IP Catalog	> processing_system7_0 (ZYNQ7 Processing System:5.5)	processing_syste	
✓ IP INTEGRATOR		Search: Q-z (9 matches)	DDR +
Create Block Design	Properties 2 D B X	Clocking Wizard	M AXI GP0 +
Open Block Design		F ILA (Integrated Logic Analyzer)	FCLK_CLK0
Generate Block Design		MicroBlaze	FCLK_RESET0_N
contrate product boorgin	Select an object to see properties	MicroBlaze Debug Module (MDM)	Our france in
✓ SIMULATION	Tel Consolo y Massanas Los Poporte Docias Pune	MicroBlaze MCS	2 0 0
Run Simulation	Consule X messages Log Reports Design Runs	SelectIO Interface Wizard	: _ L L
	Q. ≟ ≑ II 🗉 🖩 🖬	warp initializer	
Y RTL ANALYSIS	INFO: [IP_Flow 19-234] Refreshing IP repositories	* XADC Wizard	^
Run Linter	☆ INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'F:/.	Vilinx/Vi	
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, open Elaborator Brongh	update_compile_order -fileset sources_1	100 (Joure	
✓ SYNTHESIS	startgroup	untraw? + E	
Run Synthesis	endgroup	vacen/.o.	
Onen Synthesized Design			
 Open synthesized besign 	· <		Activate Windows
	Type a Tcl command here	ENTER to select, ESC to cancel, Ctrl+Q for IP details	Go to Settings to activate Windows.
Plock processing system7 0			



Step 13: Double click on the Block "processing_system7_0", to configure related parameters

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Designer Assistance available. Run Block Automation	
DDR + FIXED_IO + M_AXI_GP0_ACLK ZYNQ FCLK_CLK0 FCLK_RESET0_N	Î
	η.

Step 14: On the image mentioned below green color are editable.





Step 15: The PS-PL interface uses AXI for data interaction between PS and PL. We'll keep the default settings for now and configure it in later chapters.

🝌 Re-customize IP			×
ZYNQ7 Processing Sys Documentation Pres	stem (5.5) ets 📄 IP Location 🔅 Import XPS Settings		4
Page Navigator —	PS-PL Configuration		Summary Report
Zynq Block Design	← Q ≚ ♦		
PS-PL Configuration	Search: Q-		
Perinheral I/O Pins	Name	Select	Description
r enprierai i/o r ins	> General		
MIO Configuration	> AXI Non Secure Enablement	0 🗸	Enable AXI Non Secure Transaction
	> GP Slave AXI Interface		
Clock Configuration	> HP Slave AXI Interface		
DDR Configuration	> ACP Slave AXI Interface		
	> DMA Controller		
SMC Timing Calculation	> PS-PL Cross Trigger interface		Enables PL cross trigger signals to PS and vice-versa
Interrupts			

Step 16: Next, click on 'Peripheral I/O Pin'. When setting up PS peripherals in ZYNQ, the options can be overwhelming. Certain pins, like 16-27, can switch between Enet0 or SD0/SD1 functions, but you can only choose one. Check the schematic or user manual to decide which configuration fits best





Step 17: The serial port connects to MIO48-MIO49 on the PS. Enable UART1 (MIO48 MIO49) in the 'Peripheral I/O Pins' options. PS MIO is split into two banks: Bank 0 (BANK500) uses 3.3V LVCMOS, and Bank 1 (BANK501) uses 1.8V LVCMOS, as shown in the schematic diagram

A. Re-oustomize IP																			12
ZYNQ7 Processing System (5.	5)																		1
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Page Navigator -	Pertpheral IO Pins																	Şumm	any Report
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MIC Configuration	USB 1														-		3.15	-	
Clock Configuration	0 00 0		-	800						300					1.0	800			
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DDH Configuration	> 🖂 SPIO		570		me				-	-	1	_						1	
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Interrupts	> UARTO			LIANTO		UARTO	-	LINATO		UNRTE		LARTS		-		-			
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Step 18: Next configuration QSPI. select Quad SPI Flash in that click on Single SS 4-bit IO.

Page Navigator —	Peripheral I/O Pi	ns																S	umm	hary F	Repo
Zynq Block Design	← Q 품 €	•																			
PS-PL Configuration	Search: Q-																				
Peripheral I/O Pins				Bank 0	LVC	MOS	3.3V	~					Bar	nk 1	LV	смо	S 1.8	3V	~		
MIO Configuration	Peripherals	0	1 2 3 Quad S	4 5 6 SPI Flash	7	8	9	10	11	2 13	14	15	16	17	18	19	20	21	22	23	24
Clock Configuration	Single SS		Single	SS 4bit IO																	
DDR Configuration	O Dual Quac		ss_b	,	Ľ																
SMC Timing Calculation	O Dual Quac		Dual Quad S	SPI (8bit)			Du	al Qu	ad SP	(8bit)											
omo mining calculation	Feedback					fb															
Interrupts	> SRAM/NOR F			SRA	M/NO	R Flasi	1														s
	> NAND Flash	CS			NA		ash														
	> Ethernet 0																	En	et0		
	> Ethernet 1																				
	USB 1																				



Step 19: Configure Ethernet. The terminal is designed with an Ethernet interface, which can be selected according to the schematic diagram.

ZYNQ7 Processing Sy	stem (5.5) sets 🕞 IP Location 👎	¢F In	nport	XPS	Settin	gs																					
Page Navigator —	Peripheral I/O P	ins																						Sum	ımar	y Rej	port
Zynq Block Design	← Q ±	\$	0																								
PS-PL Configuration	Search: Q-																										
Peripheral I/O Pins					Bank	k 1	LV	смо	DS 1.	BV	~																
MIO Configuration	Peripherals	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
Clock Configuration	Single SS																										—
DDR Configuration	🔿 Dual Quac																										
SMC Timing Calculation	O Dual Quac)																									
nterrupts	> SRAM/NOR F													BRAM	NOR	Flas	h ada	110-2	41								_
	> NAND Flash	5	-	_	_	-	_	_	-	_	_	_		51 (5 (10)	Mon	1105	1, 000	110.2	-1	_	_	_	_	_	-	_	-
	✓ ✓ Ethernet 0	С								En	net0																
	MDIO																										
	> Ethernet 1																					En	et1				
	USB 0																					US	3B0				
	USB 1	<																							Ad	tiv	ate

Step 20: Expand the Ethernet 0 and Select MDIO. After selecting you can MDIO in green color as shown in the below image.

Page Navigator —	Peripheral I/O Pir	IS																					Su	ımma	ary Rep
Zynq Block Design	← Q ¥ 4	€ (Ð																						
S-PL Configuration	Search: Q-																								
eripheral I/O Pins																									
IIO Configuration	Peripherals	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	EMI
lock Configuration	Single SS																								
DR Configuration	O Dual Quac																								
MC Timing Calculation	Feedback	_																						_	
terrupts	> SRAM/NOR F	-		_							-														
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	 ✓ ✓ Ethernet 0 																							_	EMI
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	> Ethernet 1																						-		

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Step 21: To Configuration USBO by selecting the USBO as show in the below image.



Step 22: In addition to QSPI, ZYNQ can also boot from an SD card. Choose SD 0 and configure it for



∨ 🖉 SD 0	DO												s	DO											EMIO
🕑 Card Dete	3	1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	EMIO
🗌 Write Prote	3	1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	48	47	48	49	50	51	52	53	EMIO
Power Cor	Г	٦	32		34		36		38		40		42		44		48		48		50		52		
> 🗌 SD 1	Ľ	ľ					SI	D1											S	D1					EMIO
> 🗌 SPI 0				mos							SI	P10				mos									EMIO
> C SPI 1				÷												÷									\ctivat

Step 23: In GPIO mode on the PS, we can utilize the remaining unallocated MIO pins as general-purpose I/O. Select MIO46 for USB PHY reset in the GPIO MIO configuration. At this point, the peripheral configuration is completed

V 🗹 GPIO MIO	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	48	47	48	49	50	51	52	53	
Ethernet P	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	48	47	48	49	50	51	52	53	
USB PHY I	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	48	47	48	49	50	51	52	53	
I2C PHY R	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	48	47	48	49	50	51	52	53	
GPIO EMIO	<													(/	ctivate



Step 24: Next MIO Configuration.

In MIO Configuration. Ensure that Enet0 operates at LVCMOS 1.8V with a fast speed setting and enable Pullup. These parameters are crucial; failure to adjust them may lead to network connectivity issues. Keep other settings as default.

Page Navigator -	MIO Coefiguration									Summary	Report
Zing Block Design	Bank D VO Voltage LVCM	09.3.3V 🗸	Ba	nk 1 VO Vota	PPP LVCMOS 1.8V	*					
PS-PL Configuration	+ Q ± +										
Neripheral VO Pins	Search: Q-										
80 Configuration	Periphecal V 30 Peripherals	10		Signal	IO Type		Speed	1	Pullup	Direction	Polar
Diock Configuration	- SENETO	MIO 16 27									
DR Configuration	> MDIO	MIO 52 . 53	~				-	_			
NO Tanina Colordation	Enet 0	MO 15		b_dk	LVCMOS 1.8V	~	fast	~	enable 🗸	out	
arc Imang Carcolaton	Enet 0	MO 17		tect[0]	LVCMOS 1.8V	~	fast	~	← eldene	out	
nterrupts	Enet 0	MO 18		\$12(1)	LVCMOS 1.8V	¥	tast	~	enable ~	out	
	Enet 0	MO 19		bid(2)	LVCMOS 1.8V	- W	fast	~	enable ~	out	
	Enet 0	MO 20		bc(\$3)	LVCMOS 1.8V	~	fast	\sim	enable 😔	out.	
	Enet 0	MO.21		0_05	LYCMOS 1.8V	\sim	fast	~	enable 🛩	out	
	Enet 0	MO 22		ex_dR	LVCMOS 1.8V	~	fast	÷	enable 🛩	in .	
	Enet 0	MO 23		rxd[0]	LVCMOS 1.8V	~	tast	~	enable ~	in	
	Enet 0	580 24		red[1]	LVCMOS 1.8V	Ŷ	fast	*	enable 🛩	in	
										1	

Step 25: Next, proceed to the clock configuration. Ensure that the CPU and DDR values match those shown in the image below.

Page Navigator —	Clock Configuration				
Zynq Block Design	Basic Clocking Advanced Clo	ocking			
PS-PL Configuration	Input Frequency (MHz) 33.33333	3 🛞 CP	U Clock Ratio 6:2:1	~	
Peripheral I/O Pins	← Q 풒 ≑ щ				
MIO Configuration	Search: Q-				
Clock Configuration	Component	Clock Source	Requested Frequ	Actual Frequency(Range(MHz)
Clock Conliguration	 Processor/Memory Clocks 				
DDR Configuration	CPU	ARM PLL 🗸	666.666666 🛞	666.666687	50.0 : 767.0
SMC Timing Calculation	DDR	DDR PLL 🗸	533.33333 🛞	533.333374	200.000000 : 534.000000
Sille Timing Calculation	 IO Peripheral Clocks 				
Interrupts	SMC	IO PLL	100	10.000000	10.000000 : 100.000000
	QSPI	IO PLL 🗸	200 🛞	200.000000	10.000000 : 200.000000
	ENET0	IO PLL 🗸	1000 Mbps 🗸 🗸	125.000000	
	ENET1	IO PLL	1000 Mbps	10.000000	
	SDIO	IO PLL 🗸 🗸	100 🛞	100.000000	10.000000 : 125.000000
	SPI	IO PLL	166.666666	10.000000	0.000000 : 200.000000
	> CAN				
	V PL Fabric Clocks				
	FOLK CLK0	IO PLI 🗸 🗸	50 🚳	50.000000	0 100000 - 250 000000



Step 26: Change the model number to "MT41J256M16 RE-125", leave other settings as default, and click OK. This completes the core configuration of ZYNQ so far.

Page Navigator —	DDR Configuration		Summary Rep
Zynq Block Design	Enable DDR		
PS-PL Configuration	← Q ¥ ≑		
Peripheral I/O Pins	Search: Q-		
MIQ Configuration	Name	Select	Description
Nilo Coniguration	 DDR Controller Configuration 		
Clock Configuration	Memory Type	DDR 3	 Type of memory interface. Refer to UG585 Zynq Technical Reference Ma
DDR Configuration	Memory Part	MT41J256M16 RE-1:	Memory component part number. For unlisted parts choose "Custom". T
_	Effective DRAM Bus Width	32 Bit	 Data width of DDR interface, not including ECC data width. Refer to UG5
SMC Timing Calculation	ECC	Disabled	Enables error correction code support. ECC is supported only for an effe
Interrupts	Burst Length	8	 Minimum number of data beats the controller should use when communication
	DDR	533.333333	Memory clock frequency. The allowed freq range is (200.000000 : 534.00)
	Internal Vref		Enables internal voltage reference source. Disable to use external Vref p

Step 27: Click "Run Block Automation" in Vivado. The software will automatically complete some tasks related to exporting ports.

Diagram × Address Editor ×
$\textcircled{\textbf{Q}} \textcircled{\textbf{Q}} \fbox{\textbf{X}} \fbox{\textbf{X}} \textcircled{\textbf{Q}} \textcircled{\textbf{Q}} \fbox{\textbf{X}} \textcircled{\textbf{Q}} \fbox{\textbf{X}} \textcircled{\textbf{Q}} \fbox{\textbf{Y}} \fbox{\textbf{Q}} \textcircled{\textbf{Y}} \fbox{\textbf{D}} \textcircled{\textbf{D}} \fbox{\textbf{D}} \texttt{D} $
* Designer Assistance available. Run Block Automation
processing_system7_0
DDR + FIXED_IO + USBIND_0 + M_AXI_GP0_ACLK ZYNO M_AXI_GP0 + FCLK_CLK0 FCLK_RESET0_N
ZYNQ7 Processing System

Step 26: Click "by default "OK"

Make Interface External:	FIXED_IO, I	DDR		
<u>C</u> ross Trigger In:	Disable	~		
Cross <u>T</u> rigger Out:	Disable	~		
			ОК	Actiangéle V



Step28: Connect FCLK_CLKO and M_AXI_GP0_ACLK, according to save design.





Step 29: Choose "Block Design," then right-click and select "Create HDL Wrapper..." to generate a Verilog or VHDL file for the block design, creating the HDL top-level file.

Flow Navigator 😤 🚔 ? 🗕	BLOCK DE SIGN - des		Open File	Alt+O
PROJECT MANAGER	Sources × De		Open With	Þ
Add Sources	Q		Create HDL Wrapper	
Language Templates	✓ ■ Design Sourc ✓ ▲ ■ design ⊕ ■ de		View Instantiation Template Generate Output Products Reset Output Products	
IP INTEGRATOR Create Block Design	Constraints		Replace File Copy File Into Project	
Open Block Design	Source File Proper	×	Remove File from Project	Delete
Generate Block Design	🚣 design_1.bd		Enable File	Alt+Equals Alt+Minus
✓ SIMULATION Run Simulation	General Proper	C	Hierarchy Update Refresh Hierarchy	•
✓ RTL ANALYSIS	Tcl Console ×		Set as Top	P.



Keep the default options and click OK.

🝌 Create HDL Wrapper	×
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.	4
Options	
Copy generated wrapper to allow user edits	
Let Vivado manage wrapper and auto-update	
ОК	Cancel

Step 30: In the block design view, right-click and choose "Generate Output Products". This step creates essential files like IP, RTL source, and constraints for further work.



Step 31: Click on "Generate".

💫 Generate Output Products	\times
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Step 32: In the menu bar, go to "File -> Export -> Export Hardware..." This option exports hardware information, including PS terminal configuration details.



Step 33: Click Next and Finished

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Hardware design part is completed. Now we need to launch Vitis.



Create Application project

Step 1: Vitis is an independent software tool. To open Vitis, go to "Tools -> Launch Vitis" and start the Vitis software.

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Step 2: Select the previously created folder and click "Launch".

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Step 3: Click on "Create Application Project."

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Step4: Click on Next.

orm III This wizard will guide you through the 4 steps of creating new application projects. 1. Choose a platform or create a platform project from Vivado exported XSA	
 Put application project in a system project, associate it with a processor Prepare the application runtime - domain Choose a template for application to quick start development 	
Platform System Project Project	
XSA	
 A platform provides hardware information and software environment settings. A system project contains one or more applications that run at the same time. A doma provides runnine for applications, such as operating system or ISP. A workspace can contain unlimited platforms and unlimited system projects. 	
Skip welcome page next time. (Can be reached with Ba	ack button) Activate Windows

Step 5: Click on "Create a new platform hardware (XSA)". The software provides some hardware platforms for boards, but for your own hardware platform, you can choose "+".

	New Applie	ation Project	— — ×
C	Platform		
	📀 Please selec	a platform to create the project	
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Step 6: Select the previously generated XSA file in project folder and click "Open".

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Step 7: Under "Generate boot components," check the option to have the software automatically generate boot components for the project. This is usually selected by default. Click "Next."

			i hardware (X3A)	
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Step 8: Fill in the project name as "hello" and provide a project description if needed. Click "Next."

	New Application Project	
C	Application Project Details	
8	Specify the application project name and its system project	pperties
	Application project name: hello	
	System Project	
	Create a new system project for the application or sele	in existing one from the workspace 🛛 🕕
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		A chivete Mindows
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Step 9: Keep everything as it is and click "Next."

	T New Application Project			\times
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19	Select the domain that the application would link to or create a new domain Note: New domain created by this wizard will have all the requirements of the application t Select a domain	template selected in the nex Domain details	t step	
	Create new	Name	standalone_ps7_cortexa9_0	
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Step 10: In the template selection, choose "Hello World" and click "Finish."

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~	Embedded software development templates	Let's say 'Hello World' in C.	
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	OpenAMP echo-test		
	OpenAMP matrix multiplication Demo		
	OpenAMP RPC Demo		
	Peripheral lests		
	Tune DRAM tests		
	Zyng DRAM tests		
	Zynd F3BL		

Step 11: After completion, you will see that the projects have been generated.



Step 12: Double-click on the .spr file in design_1_wrapper.



Step13: Click to open the Board Support Package (BSP). Here, you can find the peripheral drivers included in the project. Xilinx provides driver documentation and example imports within the BSP.

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Step 14: In the selected Application Project, right-click and choose "Build Project," or click the "Hammer" button on the menu bar to compile the project.

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Step 15: Connect the JTAG line to the development board and the UART or USB line to the PC.
Step 16: Use PuTTY, a software that serves as a serial port terminal debugging tool.
Step 17: Click on "Run As" and select "Launch Hardware (Single Application Debug)."

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Step 18: Observe PuTTY software at this time. You should see the output "Hello World."



Step 19: For reliable system debugging, it's recommended to right-click on "Run As -> Run Configuration."

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Inside the configuration, you will find "Reset entire system" selected by default, similar to Vitis. If your project includes PL design, ensure to also select "Program FPGA" for complete functionality.



Step 20: Apart from "Run As," there's also "Debug As" available. This allows you to set breakpoints and execute single-step debugging. Click on debug and select "Launch Hardware (Single Application Debug."

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Step 21: After debugging, you can view the breakpoints you have set.

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